AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method comprising:

determining a power state of a first system, the power state to be one of at least a first and second power states,[[,]] the second power state to consume less power than the first power state; and

in response to the system being in the second power state, switching, without using a main operating system, a parallel Advanced Technology Attachment (PATA) link from the first system to a link with an autonomous subsystem.

2. (Currently Amended) The method ~~according to~~of claim 1, wherein the power state ~~is power state of~~ comprises an Advanced Configuration Power Interface Specification (ACPI) state.

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The method ~~according to~~of claim 2, wherein[[:]] if the ACPI state is S0, S1, or S2 then the PATA is switched to the first system,[[;]] and if the ACPI state is S3, S4, or S5 then the PATA is switched to the subsystem.

6. (Currently Amended) The method ~~according to~~of claim 2, wherein[[:]] if the

ACPI state is S0, or S1 then the PATA is switched to the first system,[[;]] and if the ACPI state is S2, S3, S4, or S5 then the PATA is switched to the subsystem.

7. (Currently Amended) A machine-readable medium having stored thereon data representing sets of instructions[[,]] which, when executed by a ~~processor~~machine, ~~causes said processor~~cause the machine to ~~perform the following~~:

determine a power state of a first system, the power state to be at least one of a first and second power states, the second power state to consume less power than the first power state; and

in response to the system being in the second power state, switch, without using a main operating system, a parallel Advanced Technology Attachment (PATA) link from the first system to a link with an autonomous subsystem.

8. (Canceled)

9. (Currently Amended) A system comprising:

a memory;

a Parallel Advance Technology Attachment (PATA) device connected to the memory and to a switch; and

~~a~~ the switch to

connect the system to the PATA device when the system is in a first power state, and ~~the switch to~~

connect an autonomous subsystem to the PATA device, without using a main operating system, when the system is in a second power state, the second power state to ~~conusme~~ consume less power than the first power state.

10. (Currently Amended) The system of claim 9, wherein the switch connecting the PATA device alternately connects ~~does not connect both~~ the system and the subsystem to the PATA device~~simultaneously~~.

11. (Previously Presented) The system of claim 9, wherein the switch operation is controlled by signals from the system.

12-15. (Cancelled)

16. (New) The machine-readable medium of claim 7, wherein the power state comprises an Advanced Configuration Power Interface Specification (ACPI) state.

17. (New) The machine-readable medium of claim 16, wherein if the ACPI state is S0, S1, or S2 then the PATA is switched to the first system, and if the ACPI state is S3, S4, or S5 then the PATA is switched to the subsystem.

18. (New) The machine-readable medium of claim 16, wherein if the ACPI state is S0, or S1 then the PATA is switched to the first system, and if the ACPI state is S2, S3, S4, or S5 then the PATA is switched to the subsystem.

19. (New) An apparatus comprising:

a Parallel Advanced Technology Attachment (PATA) device connected to a switch; and

the switch to

connect the system to the PATA device when the system is in a first power state, and

connect an autonomous subsystem to the PATA device, without using a main operating system, when the system is in a second power state, the second power state to consume less power than the first power state.

20. (New) The apparatus of claim 19, wherein the switch connecting the PATA device only connects to either the system or the subsystem.

21. (New) The apparatus of claim 19, wherein the switch operation is controlled by signals from the system.